EIC AC LGAD R&D Proposal

1 Introduction

AC-coupled Low-Gain Avalanche Diode (LGAD) is a new silicon sensor technology. Signals produced by charged particles in the sensor active volume are amplified via an internal p+ gain layer near the sensor surface. Signals induced on a continuous resistive n+ layer on top of the p+ gain layer, are AC coupled to patterned metal readout electrodes, which are on the sensor surface and separated by a dielectric layer from the n+ layer. The internal signal amplification and thin active volume enables precise timing measurement, while charge sharing among neighboring electrodes can provide precise position measurement. The AC-LGAD technology has been suggested to use for particle identification, tracking, and far-forward detectors at EIC where precision timing and spatial measurements are needed.

1.1 Requirements by EIC

Large-area LGAD detectors with 1.3×1.3 mm^2 pixel electrodes are being constructed for the CMS and ATLAS experiments at the HL-LHC. These detectors provide a timing resolution of 40-50 ps and a position resolution of $1.3/\sqrt{12}$ mm per hit without charge sharing. Compared to the HL-LHC, particle multiplicity and irradiation levels are much smaller at the EIC. Therefore the requirement on the minimum number of readout channels per unit area and irradiation tolerance can be relaxed. On the other hand, the timing and position resolution and material budget can be more demanding for particle identification and tracking detectors at the EIC. Specifically, low-momentum particle identification in the barrel region inside a high magnetic field requires the placing of a Time-of-Flight (ToF) layer with low material budget right behind MAPS tracking layers, while large-area ToF layers with good timing resolution are required for relatively high-momentum PID reach in the forward and backward directions. The ultimate physics requirements at the EIC for timing resolution per track is around 30 ps in the barrel region, and 20 ps in the endcap. If such AC-LGAD layers are also used for precise tracking, they would need to provide comparable or better position resolution than MAPS or MPGD detectors. The table below summarizes the proposed AC-LGAD detectors and their specific design goals at the EIC.

	Time resolution / hit	Position resolution / hit	Material budget / layer
Barrel ToF (Tracker)	<30 ps	(3-30 μm for Tracker)	$< 0.01\ X_0$
Endcap ToF (Tracker)	<25 ps	(30-50 μm for Tracker)	e-direction $< 0.05 X_0$ h-direction $< 0.15 X_0$
Roman Pots	<50 ps	$< 500/\sqrt{12}\ \mu m$	N/A
B0	<50 ps	$O(50)\ \mu m$	$< 0.01\ X_0$

Using the same or similar AC-LGAD sensors, ASICs, readout electronics, and services for these detectors, where possible, can be very cost effective, therefore this R&D effort aims at finding common technical solutions to challenges that are common across the various proposed sub-systems. Below we describe the R&D needs to achieve such a goal so that full technical designs and key components for these detectors will be available at the end of the R&D phase.

1.2 R&D Needs

The ongoing efforts and R&D needs to develop full detector designs can be categorized in 3 main areas: sensors, electronics, and system design (including cooling, engineering, and construction). These categories are detailed below.

- **Sensor:** A position resolution of a few microns from small-size AC-LGAD sensors with 100 μm pitch has been demonstrated. On the other hand, extensive R&D is ongoing at several institutes in the LGAD Consortium and internationally, by reducing the active volume thickness and optimizing implantation parameters, so that a time resolution below 20 ps per hit can be achieved. The Consortium aims at developing the technology further and reach a level of maturity so that large-size AC-LGAD sensors can be reliably made for EIC detectors. A challenge that requires targeted R&D efforts for the application of large-area ToF/tracking is to achieve high timing and position resolution while maintaining a reasonable number of readout channels per unit area and thus material budget. One such R&D effort, which is targeted at the EIC but can have broad applications, is to develop long strip AC-LGAD sensors. By increasing the length of the metal strips, the number of readout channels per unit area and thus material budget can be significantly reduced. By reducing the pitch of the strips, the position resolution in the direction perpendicular to the strips can be improved. The latter can help to achieve the position resolution needed for precise tracking layers. Another approach is an extension of the standard square pixel (e.g., 1.3×1.3 mm^2) into a long rectangular pixel (e.g., 0.5×2.6 mm^2) with high position resolution only in one direction. Rectangular pixels should maintain the same timing performance as square pixels and can share the same readout schemes, services etc.

- **Electronics:** The needs for fast timing performance and finer granularity pose significant challenges to the readout electronics and specifically to the ASIC readout chips. Present ASIC chips designed for CMS and ATLAS timing detectors have a jitter on the order of 20–30 ps, and a pixel granularity of 1.3×1.3 mm^2. Reduced granularity and better timing resolution requirement will make it more challenging to fit all the circuit components within the available space, and also likely lead to significantly increased power consumption due to increased total number of channels. The Consortium will collaborate on addressing these challenges. For example, the IJCLAB (Orsay)/ Omega, Ecole Politechnique (Saclay) group is developing a new ASIC with a pitch size of 0.5×0.5 mm^2 that meets the requirements set by the EIC Roman Pot detector, and is providing in-kind labor and material contributions. The ASIC uses the current ATLAS chip (ALTIROC) design with the 130 nm node technology as a stepping stone. The design is advanced with a first submission planned for FY22, which is fully supported by French funds. In future FYs the IJCLAB/Omega group will keep seeking funds from French funding agencies to continue such an effort for further required prototype and full-size ASIC iterations, but such funds are not currently secured. A discussion among the institutes participating in the LGAD Consortium and the recruiting of further ASIC designers with expertise in fast-time electronics will start immediately to evaluate a common development of an ASIC that serves both Roman Pots and ToF, or to evaluate how the ASIC designs for EIC Roman Pots and for CMS/ATLAS ToF can be leveraged for the EIC ToF ASIC development. For the development of such an ASIC further resources are expected in fiscal years beyond FY22 to expand the R&D and meet the stringent jitter, fine granularity, and power consumption requirements of a large-area ToF detector. The Consortium will work on understanding the requirements, developing the chips, and addressing related problematics, e.g. clock jitter and distribution, power consumption etc., based on their established expertise and development of flexes, interconnects and electronics for HL-LHC timing detectors.

- **System design, cooling, engineering, and construction:** Constructing a full-scale detector requires significant work on the system-level design, prototyping, and engineering. The key elements include the light-weight mechanical structure for the barrel ToF, and the cooling system, most notably for the large-area endcap ToF detectors. Several demonstrators with increasing capabilities and dimensions are planned during the course of this effort. Members of the group have been involved in the construction of many large-scale experiments at HERA, RHIC, SLAC, Jefferson Lab, and the (HL-)LHC. In particular, the Consortium plans to apply its members' experience with LGAD-based timing detectors developed for CMS and ATLAS experiments to the construction of high-performance, cost-effective EIC detectors.

The **timeline** of the effort is outlined here below.

1. In **FY22** the effort will focus on defining the physics and performance requirements of the sub-systems that plan to use AC LGADs and identify common areas of R&D needed. The

already established sensor development will focus on achieving ~ 20 ps intrinsic time resolution of pixel and/or long strip sensors. The ASIC design effort will ramp up, focusing initially on the achievement of a 30 ps time resolution and a pixelation of 500 μm.

2. In **FY23** the effort will shift to achieving a time resolution in the range 25-30 ps per hit (sensor+ASIC) and will start tackling the pressing issue of cooling and light-weight mechanical design. In parallel, the sensor and ASIC prototypes will undergo several tests and further development to meet the stringent requirements of the ToF/tracking sub-system.

3. In **FY24** ASICs that meet the ToF requirements will be prototyped, while the whole mechanical and electronics design, including flexes and off-detector electronics will be developed.

4. In **FY25-26** the effort will focus on the optimization of sensors and electronics, and the full demonstration of an advanced module-size prototype.

2 Plan for FY22

Here follows the list of **Milestones** for FY22:

1. **June 2022**: Definition of physics and performance specifications for different sub-systems, with a focus on detector layouts, material budget requirements, timing, and space resolution targets.

2. **June 2022**: Sensor prototypes that meet space resolution specifications of the various subsystems and have a time resolution of 20-30 ps.

3. **Sept. 2022**: A prototype ASIC design to readout AC LGADs using signal sharing across neighboring electrodes and has 30 ps time resolution with low power consumption.

Here follows the list of **Deliverables** for FY22:

- High-level strawman layout design and requirements for AC-LGAD detectors by June 2022.
- Production of thin (20, and 30 μm) sensors for ToF application with time resolution ~ 20 ps by BNL Instrumentation (IO). Expected production start/end dates are Oct. 2021/Feb. 2022.
- Production of medium/large-area sensors with different doping concentration, pitch, and gap sizes between electrodes to optimise performance by BNL IO and Hamamatsu. BNL production start/end dates are Feb. 2022/June 2022. Expected date for the Hamamatsu production submission is July 2022. The delivery date of wafers and diced sensors will depend on the international availability of silicon and on the vendor time scale, but it is expected by March 2023.
- Sensor testing at BNL, UIC, and LANL using laser and β sources as soon as sensors become available, and will continue through the year. Beam tests are reserved at FNAL for Spring 2022.
- A first ASIC prototype that is compatible with EIC Roman Pot requirements and can read out an AC LGAD with ~ 500 μm pitch and ~ 30 ps time resolution. Expected date for the submission to the foundry is February, 2022. The date of wafer/chip delivery will depend on the international availability of silicon and on foundry time-scale but it is expected by the end of summer 2022.
- Formation of a team of experts to start developing the cooling strategy and identifying mechanical requirements by May 2022.
- Formation of a team of experts to start developing strategy for flexes, interconnects, and off-detector electronics by July 2022.

Tables below summarise the current estimate of M&S and labor needed in FY22.

Vendor/ Institute	M&S Item	Cost per Item [$]	N. Items	Tot. Cost [$]
BNL IO	Sensor fabrication (incl. labor)	50k (10 wafers)	1.5	75k
Hamamatsu	Sensor fabrication (incl. labor)	75-100k+3-5k/wafer	0.3	32k(+16k in-kind)
IJCLAB/Omega	ASIC submission	N/A	1	0 (in-kind)
Multiple	1-4 channel fast-time test-board	100	40	4k
Multiple	Multi-channel fast-time test-board	300	20	6k
BNL	Travels to Fermilab testbeam	2k	2	4k
UIC	Travels to Fermilab testbeam	1k	2×2	4k
Rice	Travels to BNL and Fermilab	3k	2	6k
UCSC	Travels to Fermilab	3k	1	3k
TOT.				134k

Inst.	Task	Labor Type	FTEs [%]	Cost [$]
Multiple	Testboard part assembly and testing	El. Tech.	10	20k
BNL	Sensor+testboard assembly (incl. wirebonds)	El. Tech.	10	20k
	Sensor dicing & testing before distribution	Tech.	15	0 (in-kind)
	Sensor testing	Scientists	20	0 (in-kind)
	Sensor testing	Postdocs	20	0 (in-kind)
IJCLAB/ Omega	ASIC design	Engineers	20	0 (in-kind)
	ASIC design	Scientists	90	0 (in-kind)
	ASIC design	Students	80	0 (in-kind)
UIC	Detector simulation, strip sensor device simulation and design optimization	Faculty	15	0 (in-kind)
	Strip sensor dicing & testing before assembly	Tech./Stud.	15	15k
	Sensor+testboard assembly (incl. wirebonds)	El. Tech.	10	15k
	Detector simu., sensor bench/testbeam test	Postdoc/Sp.	50	45k
Rice	Detector simulation	Faculty	10	0 (in-kind)
	Pixel sensor testing, thin sensor optimization	Postdoc	50	50k
	Sensor testing	Students	20	0 (in-kind)
UCSC	General oversight, data analysis	Faculty	10	0 (in-kind)
	Testbeam operations, data analysis	Postdocs	10	0 (in-kind)
	Testbeam apparatus design and production, sensor testing	Specialists	15	32k
	Test beam execution, data analysis	Students	15	4k
LANL	Sensor testing	Scientists	20	0 (in-kind)
	Sensor testing	Postdocs	20	15k
TOT.				216k

3 Deliverable and Milestones for FY23-26

- **FY23 Q1-Q2**: Continue laboratory tests with FY22 sensors and ASICs.
- **FY23 Q1**: Design and submission for fabrication of advanced sensor prototypes with 20-30 ps time resolution and space resolution that matches Roman Pots, ToF, and Tracker requirements. This sensor design will be used as baseline for the CD2 review.
- **FY23 Q1**: Development of a general cooling strategy and mechanical requirements to be used as baseline for the CD2 review.
- **FY23 Q1**: Development of a general layout of flexes and off-detector electronics to be used as baseline for the CD2 review.
- **FY23 Q1**: 2nd ASIC prototype design and submission with better performance and extended features. This design will be used as baseline in the CD2 review.
- **CD2 - January, 2023.**

- **FY23 Q2**: Procurement of prototype flexes, interconnects, and off-detector electronics.
- **FY23 Q3**: Sensor + ASIC demonstrator for EIC applications and testing with particle beam.
- **FY23 Q4**: Irradiation campaign for sensor and ASIC prototypes.
- **FY23 Q3-4**: Laboratory testing of new available sensors and ASICs.
- **FY23 Q4**: Sensor batch submission with optimised sensor layouts and performance, based on laboratory and test-beam results. This sensor design will be used as baseline for the CD3 review.
- **FY24 Q2**: Third ASIC submission, aiming to match ToF timing requirements. This ASIC design will be used as baseline for the CD3 review.
- **FY24 Q2**: Cooling demonstrator and building of a mechanical module. This will be used as baseline for the CD3 review.
- **FY24 Q2**: Advanced design and prototyping of flexes, interconnects, and off-detector electronics. This will be used as baseline for the CD3 review.
- **CD3 - March, 2024.**
- **FY24 Q3-4**: Laboratory testing of new available sensors and ASICs.
- **FY25**: Module-size sensor fabrication with target time and space performance.
- **FY25**: Full-scale ASIC submission.
- **FY25**: Development of final cooling system.
- **FY25**: Production of flexes, interconnects, and off-detector electronics with final design.
- **FY26**: Final full-scale ASIC submission with optimized and final design.
- **FY26**: Building of a fully electrical module with optimised sensor, ASICs, flexes, interconnects, and cooling.